

## **REMARKS**

Claims 1-3, 5-10, 12-17, 19-21, and 63-72 are pending. The Examiner rejected the independent claims under 35 U.S.C. 103(a) as being unpatentable over Paul (2005/0047334) in view of Aimoto (6,144,636). Claims 4-8, 13-16, and 66 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form. Elements of dependent claim 4 have been incorporated into the independent claims 1, 63, 67, and 70. Although not all dependent and intervening claim limitations have been incorporated into the independent claims, sufficient elements of objected to dependent claim 4 are believed to have been incorporated to place the independent claims in condition for allowance.

Independent claims 1, 63, and 67 now recite “wherein the first instruction, having a source identifier field corresponding to the destination node and a destination identifier field corresponding to the source node, reduces transmissions at the first intermediate switch and the second instruction reduces transmissions at a plurality of switches including the first intermediate switch.” Claim 70 recites “wherein the edge quench frame has a source identifier field corresponding to the system and a destination identifier field corresponding to the source node.”

Paul states “The header includes a 24 bit source identifier (S\_ID) that identifies the source for the frame, as well as a 24 bit destination identifier (D\_ID) that identifies the desired destination for the frame. These port identifiers are uniquely assigned to every node in a Fibre Channel fabric. Under the standard Fibre Channel switch fabric addressing scheme, each port identifier is considered to contain three 8-bit words: a domain address or Domain\_ID (bits 23-16 of the port ID), an area address or Area\_ID (bits 15-8), and a port address or Port\_ID (bits 0-7). Each switch in a Fibre Channel fabric is generally assigned a unique domain address. Groups of ports can be assigned to a single area within the switch. The addressing scheme allows 256 ports in each area, 256 areas within each switch, and 239 switches in a fabric (this is fewer than 256 switches because some switch address are reserved). The scheme allows certain routing decisions to be made by examining only a single 8-bit word. For example, a frame could be routed to the appropriate E\_Port after examining only the domain address that identifies the switch on which the destination is located.” [0006]

Aimoto states “The present invention provides a packet switch for setting a connection between a transmission source of a packet and a reception destination thereof so as to perform communication. The present invention includes a packet buffer which includes at least one input port and a plurality of output ports. An input packet from the input port is delivered to at least one output port in accordance with address information of the input packet and connection information having been set in the packet switch at the time of setting the connection between the transmission source and the reception destination. A bandwidth management packet for giving notice of a congested state of the packet switch is transferred on the connection. The present invention further includes a register which holds threshold value information for indicating an amount of use of the packet buffer that causes congestion, a counter which provides a count representative of a current amount of use of the packet buffer, a comparator which compares the count from the counter and the threshold value information from the register and outputs a result of the comparison, and a congestion decision/notification circuit which writes congestion notification information into the bandwidth management packet based on a result of the comparison by the comparator.” (column 4, lines 6-29)

However, Paul and Aimoto even if appropriately combined do not teach or suggest “wherein the first instruction, having a source identifier field corresponding to the destination node and a destination identifier field corresponding to the source node, is sent only to the first intermediate switch to reduces transmissions only at the first intermediate switch and the second instruction is sent to the plurality of switches including the first intermediate switch to reduces transmissions at a the plurality of switches including the first intermediate switch.” Similarly, Paul and Aimoto even if appropriately combined do not teach or suggest “wherein the edge quench frame has a source identifier field corresponding to the system and a destination identifier field corresponding to the source node.”

## **CONCLUSION**

In light of the above remarks, the rejections to the independent claims are believed overcome for at least the reasons noted above. Applicants' Representative believes that all pending claims are allowable in their present form. If the Examiner has any questions or concerns for Applicants' Representative, the Examiner is encouraged to contact her at the number provided below.

Respectfully submitted,  
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